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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,335	10/28/2003	Jeffrey P. Gambino	BUR920010040US2 (14574A)	4853

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EXAMINER	
RAO, SHRINIVAS H	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/695,335	GAMBINO ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *13-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

Applicants' amendment filed on April 12, 2006 has been entered and forwarded to the Examiner on April 19, 2006.

Therefore claims 13 –20 as recited in the amendment are currently pending in the Application.

Information Disclosure Statement

No further IDS after the one filed 9/27/2004 has been filed in this case.

Claim Rejections - 35 USC # 1 02

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless - (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 13-18 and 20 re rejected under 35 U.S.C. 102(b) as being anticipated by Augusto (U.S. Patent No. 5,963,800 herein after Augusto) OR Yu (U.S. Patent No. 6,787,402) (both previously applied).

With respect to claim 13 , Augusto or Yu describes a double-gated/ double channel FIN metal oxide semiconductor field effect transistor (MOSFET) comprising :

let is noted that Applicants' have ONLY recited a double-gated/ double channel FIN metal oxide semiconductor field effect transistor (MOSFETI" only in the preamble of claim 1 and all dependent claims .

Further current U.S. Law requires the recitation "a double-gated/ double channel FIN metal oxide semiconductor field effect transistor (MOSFET) " has not been given patentable weight because it has been held that a preamble is denied the effect of a Imitation where the claim is drawn to structure and the portion of the claim following the preamble is a self-contained description of the structure not depending upon for completeness upon the introductory clause . Kropa V Robie 88 USPQ478 (CCPA 1951).

Therefore the recitation "a double-gated/ double channel FIN metal oxide semiconductor field effect transistor (MOSFETI" has not be given patent able weight. a bottom Si-containing Ayer, (Augusto col. 10 lines 3-5) (Yu fig. 1 #12) an insulating region present atop said bottom Si-containing layer, (Augusto fig. 3 # 5,7 col. 1 1 lines 29-46, Flow 4- SOI substrate) (Yu fig. #14) said insulating region having at least one partial opening therein, (Augusto figure 3 # 5) (Yu col. 3 lines 25-35, 38-40- buried stack) a gate region in said partial opening, (Augusto fig. 3 # 13) (Yu figure 4, col. 3 lines 25-40) said gate region comprising two regions of gate conductor that are separated from vertical channel regions by an insulating film, (YU figure 6, col. 3 lines 60-65) (Augusto fig. 3 # 13 separated from 3 by 1 1, vertical channel- title etc.) said insulating film comprising a gate dielectric and having opposite vertical surfaces adjacent to the channel regions, (Augusto e.g. figure 3 gate insulator # 11) (Yu figures 3-5 etc.) source/drain diffusion regions abutting said gate region, (Augusto figure 3 # 5',7' (source) and # 1. (drain) abutting gate 13, col. 2 lines 38-40) (Yu figure 6 , etc. said source/drain diffusion regions having junctions that are self-aligned to the vertical

fin-shaped silicon containing channel regions and the gate region, (Augusto e.g. figure 3 # 5',7' (source) and #1',15 (drain) self-aligned with channel 3, 31) (Yu figures 3-6 etc., Abstract lines 5-6) and insulating spacers in said partial opening that separate the gate region and the source/drain diffusion N region formed orthogonal to said insulating film. (Augusto figure 3 spacer not numbered orthogonal to gates 13) (Yu figures 3-6 , etc.) and wherein said gate region is between said insulating spacers (Augusto figures) (Yu figures 6 etc. and the gate region is self-aligned to the source/drain diffusion regions and vertical channel regions. (Augusto e.g. figure 3 # 5',7' (source) and #1',15 (drain) self-aligned with channel 3, 3, col. 2 lines 38-40, col. 12 lines 41-46). (Yu figures 3-6 etc.)

With respect to claim 14 Augusto describes the Fin MOSFET of Claim 13 wherein said insulating region includes an insulating layer of an SOI material. (Augusto col. 25 lines 65-66). (Yu col.3 , line 21 etc.)

With respect to claim 15 Augusto describes the Fin MOSFET of Claim 13 wherein said partial opening exposes a portion of said insulating layer of said Sol material. (Augusto figures 9.4, 15.1,. etc.) (Yu col. 3 lines 25-35, 38-40- buried stack and col. 3 line 21-SOI).

With respect to claim 16 Augusto describes the Fin MOSFET of Claim 13 wherein said insulating film is formed surrounding a portion of a Si-containing layer. (Augusto figure 9.4, 15.1 insulators on sides) (Yu figures 3-5 etc.)

With respect to claim 17 Augusto describes the Fm MOSFET of Claim 16 wherein said gate dielectric is comprised of an oxide, a nitride, an oxy nitride or any

combination or multi layer thereof. (Augusto figure 15.1 , col. 27 lines 5-65). (Yu col.3 line 24 , etc.)

With respect to claim 18 Augusto describes the Fm MOSFET of Claim 13 wherein said regions of gate conductor are each comprised of polysilicon, amorphous Si, a conductive elemental metal, an alloy of a conductive elemental metal, a nitride or silicide of a conductive elemental metal or multi layers thereof. (Augusto col. 6 line 50 and PMOS or NMOS by definition is a metal gate, figure 8.3 etc.) (Yu col. 3 lines 46-50).

With respect to claim 20 Augusto describes the Fm MOSFET of Claim 13 wherein said source/drain diffusion regions are formed in a portion of a patterned Si-containing layer. (Augusto figure 7 (s) and (d) formed in patterned Si containing layer). (Yu figures).

Claim Rejections - 35 USC Section 1 03

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action.

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the ad to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim I9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Augusto (U.S. Patent No. 5,963,800 herein after Augusto) as applied to claims 13-18 and 20 above .

With respect to claim 19 Augusto describes the Fm MOSFET of Claim 13 further comprising silicide regions formed atop said source/drain diffusion regions. (Augusto . col. 6 line 50). (well known in the art to from silicide layers atop source/drain e.g. 5,315,144, 6,656,824)

Response to Arguments

Applicant's arguments filed 04/12/2006 have been fully considered but they are not persuasive for the following reasons.

Applicants' first contention that neither Augusto nor Yu applied references disclose/teach all recited element is not persuasive,

(a) Augusto teaches /discloses an insulator region that is located atop a bottom Si-containing layer and has at least one partial opening therein .

It is noted that Augusto teaches an embodiment in figure 3 and further clarifies that the embodiment of figure 3 includes (flow 4) as further explained with reference to figures 4 and 10.1 to 10.3 etc. having SOI (Silicon on insulator technologies) wherein an insulating layer is present over the silicon (containing) layer and lists at least 8 materials that are suitable as insulating materials. (Augusto col.14 line 50-63 reproduced below) .

present invention. Ideally, the barriers are made of an insulator, epitaxially compatible with silicon. Quite a few of these materials exist and are applied in Silicon on Insulator (SOI) planar technologies. A short list of those materials includes:

1) Al_2O_3 (Sapphire=Aluminium Oxide)
2) CaF (Calcium Fluoride)
3) CeO_2 (Cerium Dioxide)
4) AlN (Aluminium Nitride)
5) SrO (Strontium Oxide)
6) $SrTiO_3$ (Strontium Titanate)
7) $BaTiO_3$ (Barrium Titanate)
8) $SrVO_3$ (Strontium Vanadium Oxide)

Further the at least one partial opening is seen in figures 7.1 etc. (reproduced below) which is similar if not identical to Applicants' partial opening shown in Applicant's figure 6A # 32 , specification page 8 line 27) .

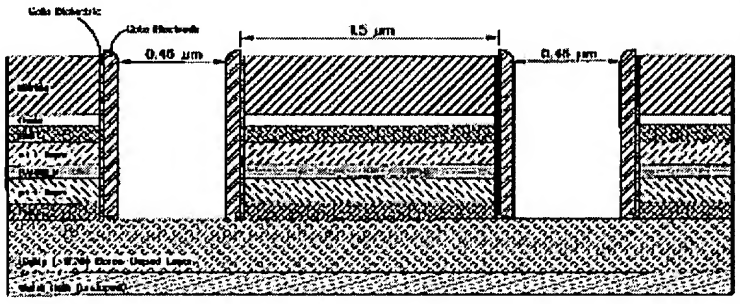

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FIG. 7.1

Applicants' second contention that Augusto fails to disclose a vertical fin –shaped silicon containing channel region is not persuasive because Applicants' arguments are not commensurate in scope with the presently recited claims for reasons stated below .

Applicants' allege that Augusta's source/drain/ channel regions although vertically arranged in relation to one another are not fin-shaped bodies, which is

different from the present claim recitation that only requires the channel region to be vertical fin shaped and the source/drain regions to can be of any shape.

Further , Applicants' allege that Augusto's source/drain/ channel regions do not stand vertically on the substrate is also not persuasive because Augusto in figure 5 (reproduced below) shows substrate (n-type wafer) on which PMOS source, PMOS drain and PNOS Channel all stand vertically.

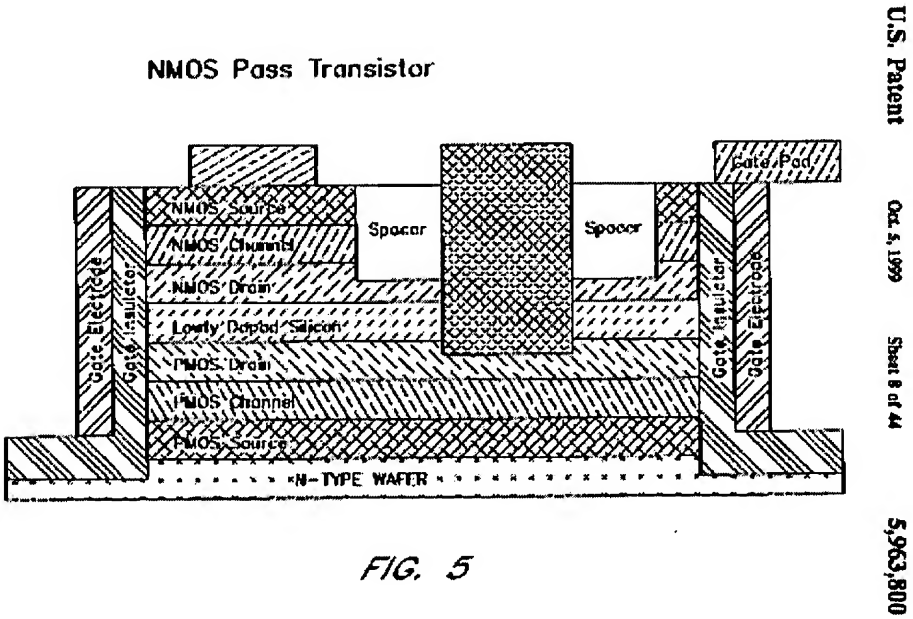

FIG. 5

It is further noted that figure 5 above shows source/ drain regions are laterally extending i.e. fin type.

Therefore Augusto and the presently claimed invention re not fundamentally different , but when fully read and understood, Augusto describes each and every element presently set forth in claims 13-18 and 20 .

It is further noted that the applied Yu reference independently also discloses each and every element presently set forth in claims 13-18 and 20, as shown above and below .

Applicants' allege the applied Yu reference fails to disclose, " an insulator region that has at least one partial opening therein " , which is not persuasive because Yu in figure1 discloses insulator 14 on substrate 12 , see also col. 3 lines 19-22 and Yu further states in col.3 lines 26-28 that a vertical channel (i.e. at least one partial opening therein) in insulator 14 is created by etching which is similar if not identical to Applicants' partial opening shown in Applicant's figure 6A # 32 , specification page 8 line 27).

Applicants' next contention that Yu allegedly fails to disclose a gate region that is located in a partial opening in an insulating region is also not persuasive because again the applicants' have misinterpreted the rejection, The correct reading of the rejection is that Yu in col.3 lines 25-40 states that a vertical channel is formed in insulating layer 14 or insulating layer when substrate is SOI in the I (insulating layer) . This vertical channel is then filled with gate material i.e. gate region is located in the partial opening in the insulating layer. Applicants' are arguing that gate material 26 is deposited over insulator layer 18 , has no bearing to vertical channel created in insulating layer 14(or SOI) in which gate material 26 is deposited , albeit over insulating layer 18.

Therefore all of Applicants' arguments with respect to Yu are not found persuasive and all claims are finally rejected.

It is further noted that the applied Augusto reference independently also discloses each and every element presently set forth in claims 13-18 and 20, as shown above.

The 103 rejection of claim 19 was alleged to be over come because of the alleged deficiencies of the applies primary Augusto reference .

However as shown above Augusto describes/teaches all of the presently recited limitations of the independent claim and dependent claim 19, therefore the Applicants' arguments do not overcome the outstanding rejection and is finally rejected.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (571)272-1718. The examiner can normally be reached on 8.00 to 5.00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fahmy Wael can be reached on (571) 272-1714. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steven H. Rao

Patent Examiner

June 14, 2006.

LONG PHAM
PRIMARY EXAMINER